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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/786,834	02/25/2004	Shigeji Ikeda	721771822	2971

7590 09/20/2005

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EXAMINER

HOANG, HUAN

ART UNIT PAPER NUMBER

2827

DATE MAILED: 09/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/786,834

Applicant(s)

IKEDA ET AL.

Examiner

Huan Hoang

Art Unit

2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1,2,6-12,14-16 and 18 is/are rejected.
- 7) ☒ Claim(s) 3-5,13 and 17 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____. | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

The Preliminary Amendment filed on 02/25/04 has been received and entered.

Drawings

1. Figures 9-12 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 10, 14 and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The recitation "wherein said memory space is divided into a plurality of memory spaces" (claims 10, 14 and 18, lines 2-3) is unclear since it is impossible to divide a memory space into a plurality of memory spaces.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 2, 11, 12, 15 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Ikabata.

Ikabata discloses a semiconductor memory device and a method for refreshing storage in a semiconductor memory device having all the elements and steps as recited in claims 1, 2, 11, 12, 15 and 16 as follows:

a refresh control circuit (column 3, lines 23-24) for performing refreshment of the information only to a submemory space (column 3, lines 47-48), which is in use when the refreshment of the information is performed, the submemory space holding the information necessary to be refreshed, selected (column 3, lines 47-48) from among a plurality of submemory spaces formed by a previous division of the memory space (column 1, lines 29-35).

The division of an address space (memory array address) in a memory space to obtain a plurality of submemory spaces each having an address (a bank address) is inherent to select a submemory space (a bank).

6. Claims 1, 2, 6-16, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Hidaka.

Hidaka discloses a semiconductor memory device and a method for refreshing storage in a semiconductor memory device having all the elements and steps as recited in claims 1, 2, 6-12, 14-16, and 18 as follows:

a refresh control circuit (column 9, lines 25-26) for performing refreshment of the information only to a submemory space (column 9, lines 50-56), which is in use when the refreshment of the information is performed, the submemory space holding the information necessary to be refreshed, selected (column 9, lines 50-51) from among a plurality of submemory spaces formed by a previous division of the memory space;

wherein the memory cell array includes a row decoder (106, Fig. 57) and a refresh counter a row decoder (104, Fig. 57), the row decoder and the refresh address counter are set to specify a row address to which the refreshment is performed in addresses of the memory cell array, and wherein the refresh control circuit is provided in the row decoder; and

the memory device further comprising a row decoder, a multiplexer and a refresh address counter connected in order (106, 105 and 104, Fig. 57).

Allowable Subject Matter

7. Claims 3-5, 13 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art does not teach or suggest the following:

wherein said refresh control circuit performs a logical product of data pertaining to whether each of said submemory spaces are in use and refresh address data to be input to each address;

wherein said refresh control circuit is inserted between said memory cell array and said row decoder; and

wherein said refresh control circuit is provided in said row decoder.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Huan Hoang whose telephone number is (571) 272-1779. The examiner can normally be reached on Mon-Fri 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2827

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Huan Hoang
Primary Examiner
Art Unit 2827

HH
9/14/05